SONY

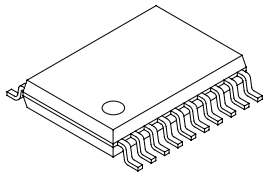
CXD3400N

6-channel CCD Vertical Clock Driver

Description

The CXD3400N is a vertical clock driver for CCD image sensor. This IC is composed of 6 channels which supports high frame rate readout mode.

20 pin SSOP (Plastic)



Features

- Composition
  - Vertical transfer output 3 levels driver × 4
  - 2 levels driver × 2
  - Electronic shutter output 2 levels driver × 1
- Suitable drive capability for high-pixel CCD (40% improved compared to current device)
- Small package (20-pin SSOP)
- 2.7 to 5.5V supported input interface

Applications

Digital still camera

Structure

CMOS

Absolute Maximum Ratings

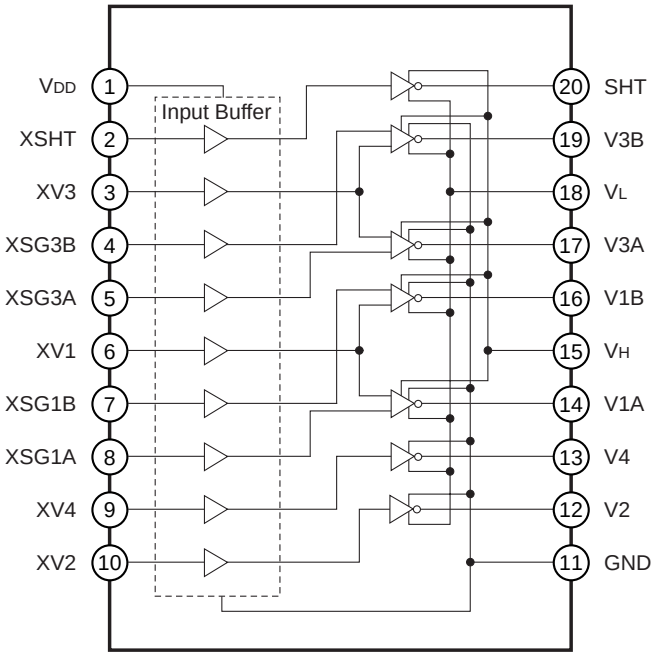
• Supply voltage	V_{DD}	GND – 0.3 to +7.0	V
• Supply voltage	V_L	GND to –10	V
• Supply voltage	V_H	V_L + 26	V
• Input voltage	V_{IN}	GND – 0.3V to V_{DD} + 0.3	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 5.5	V
• Supply voltage	V_L	–5.0 to –9.0	V
• Supply voltage	V_H	11.5 to 15.5	V
• Operating temperature	Topr	–20 to +75	°C

E98Y42A9X

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Functions
1	V_{DD}	—	Input power supply (3.3V system)
2	XSHT	I	SHT pulse input
3	XV3	I	V3A and V3B transfer pulse input
4	XSG3B	I	V3B readout pulse input
5	XSG3A	I	V3A readout pulse input
6	XV1	I	V1A and V1B readout pulse input
7	XSG1B	I	V1B readout pulse input
8	XSG1A	I	V1A readout pulse input
9	XV4	I	V4 transfer pulse input
10	XV2	I	V2 transfer pulse input
11	GND	—	GND (= V_M)
12	V2	O	High voltage output (2 levels: V_M, V_L)
13	V4	O	High voltage output (2 levels: V_M, V_L)
14	V1A	O	High voltage output (3 levels: V_H, V_M, V_L)
15	V_H	—	Positive power supply for high voltage output (15V system)
16	V1B	O	High voltage output (3 levels: V_H, V_M, V_L)
17	V3A	O	High voltage output (3 levels: V_H, V_M, V_L)
18	V_L	—	Negative power supply for high voltage output (–7.5V system)
19	V3B	O	High voltage output (3 levels: V_H, V_M, V_L)
20	SHT	O	High voltage output (2 levels: V_H, V_L)

Truth Table

Input				Output		
XV1, 3	XSG1A, 1B, 3A, 3B	XV2, 4	XSHT	V1A, 1B, 3A, 3B	V2, 4	SHT
L	L	X	X	V_H	X	X
L	H	X	X	V_M	X	X
H	L	X	X	Z	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_H
X	X	X	H	X	X	V_L

Z: High impedance X: Don't care

Electrical Characteristics

DC Characteristics (V_{DD} = 3.3V, V_H = 15V, V_M = GND, V_L = –8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH}		0.7V_{DD}	—	—	V
"L" level input voltage	V_{IL}		—	—	0.3V_{DD}	V
Input current	I_{IN}	V_{IN} = GND to 5V	–10	0.0	10	µA
Operating supply current	I_H	*1	—	0.10	0.20	mA
Operating supply current	I_{DD}	*1	—	0.25	0.50	mA
Operating supply current	I_L	*1	–8.5	–5.5	—	mA
Output current	I_{OL}	V1A, 1B, 3A, 3B, V2, 4 = –8.25V	10	—	—	mA
Output current	I_{OM1}	V1A, 1B, 3A, 3B, V2, 4 = –0.25V	—	—	–5.0	mA
Output current	I_{OM2}	V1A, 1B, 3A, 3B = 0.25V	5.0	—	—	mA
Output current	I_{OH}	V1A, 1B, 3A, 3B = 14.75V	—	—	–7.2	mA
Output current	I_{OSL}	SHT = –8.25V	5.4	—	—	mA
Output current	I_{OSH}	SHT = 14.75V	—	—	–4.0	mA

*1 See Measurement Circuit. Shutter speed 1/10000

Note) Current direction +: inflow to IC; –: outflow from IC

Switching Characteristics (V_{DD} = 3.3V, V_H = 15V, V_M = GND, V_L = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLM}	*1	50	70	100	ns
Propagation delay time	T_{PMH}	*1	50	70	100	ns
Propagation delay time	T_{PLH}	*1	50	70	100	ns
Propagation delay time	T_{PML}	*1	10	30	50	ns
Propagation delay time	T_{PHM}	*1	10	30	50	ns
Propagation delay time	T_{PHL}	*1	10	30	50	ns
Rise time	T_{TLM}	$V_L \rightarrow V_M$*1	200	350	500	ns
Rise time	T_{TMH}	$V_M \rightarrow V_H$*1	200	350	500	ns
Rise time	T_{TLH}	$V_L \rightarrow V_H$*1	30	60	90	ns
Fall time	T_{TML}	$V_M \rightarrow V_L$*1	200	350	500	ns
Fall time	T_{THM}	$V_H \rightarrow V_M$*1	200	350	500	ns
Fall time	T_{THL}	$V_H \rightarrow V_L$*1	30	60	90	ns
Output noise voltage	V_{CLH}	*2	—	—	1.0	V
Output noise voltage	V_{CLL}	*2	—	—	1.0	V
Output noise voltage	V_{CMH}	*2	—	—	1.0	V
Output noise voltage	V_{CML}	*2	—	—	1.0	V

*1 See Switching Waveform.

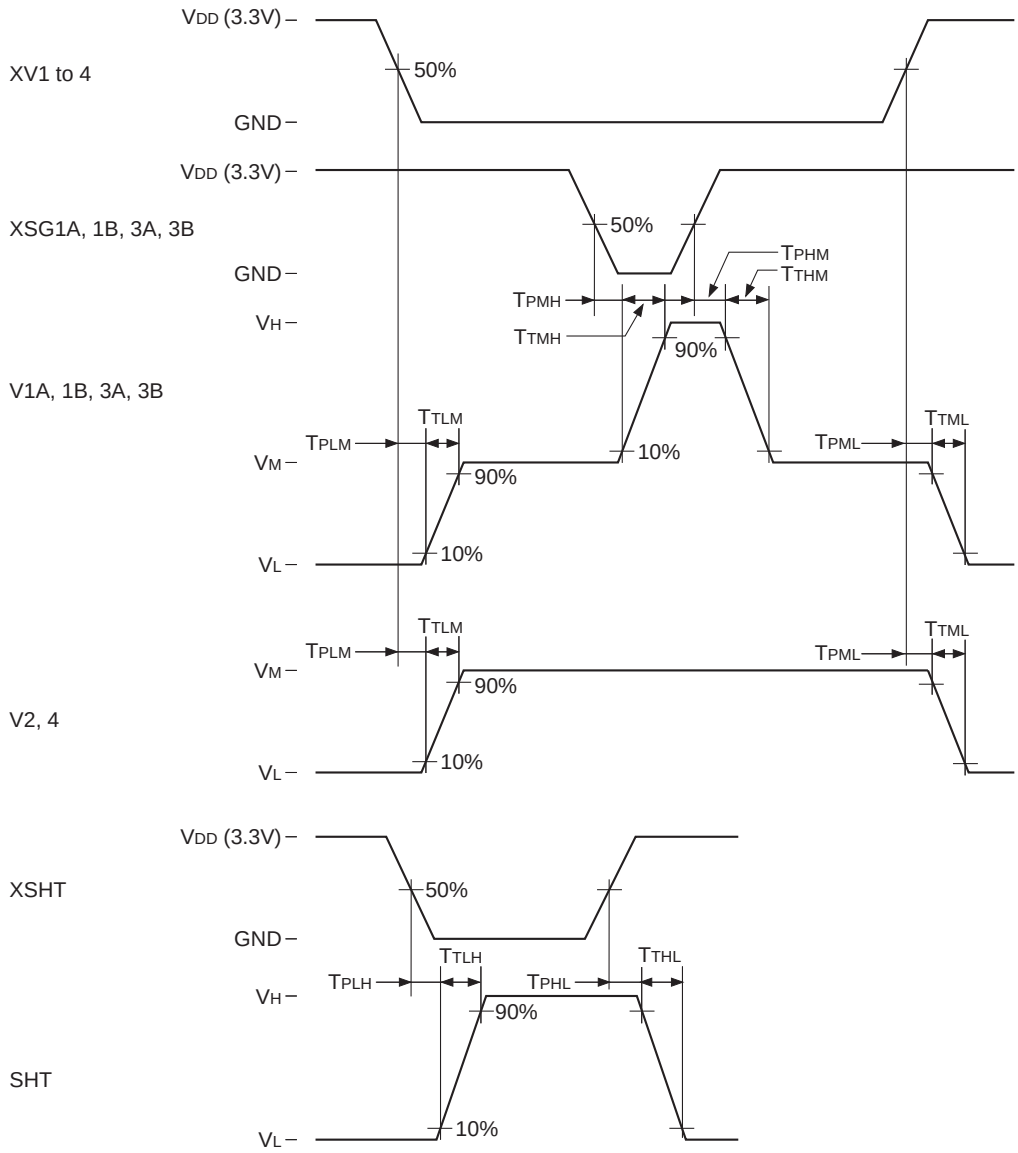
*2 See Noise on a Waveform.

Note) Each item is evaluated by Measurement Circuit.

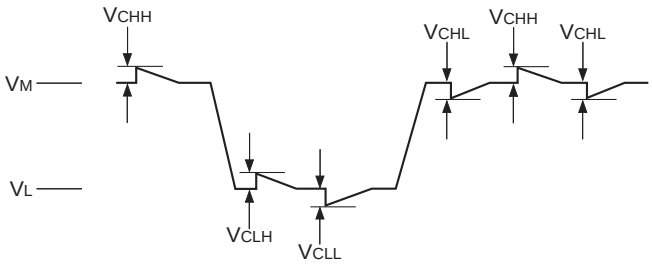
Notes on Operation (See Application Circuit.)

1. Be sure to protect against static electricity because this IC is MOS structure.
2. A bypass capacitor (0.1µF or more) is connected between GND and near each power supply (V_H, V_{DD}, V_L).
3. In order to protect CCD image sensor, input SHT pin output to SUB pin of CCD image sensor after that has been clamped at V_H.

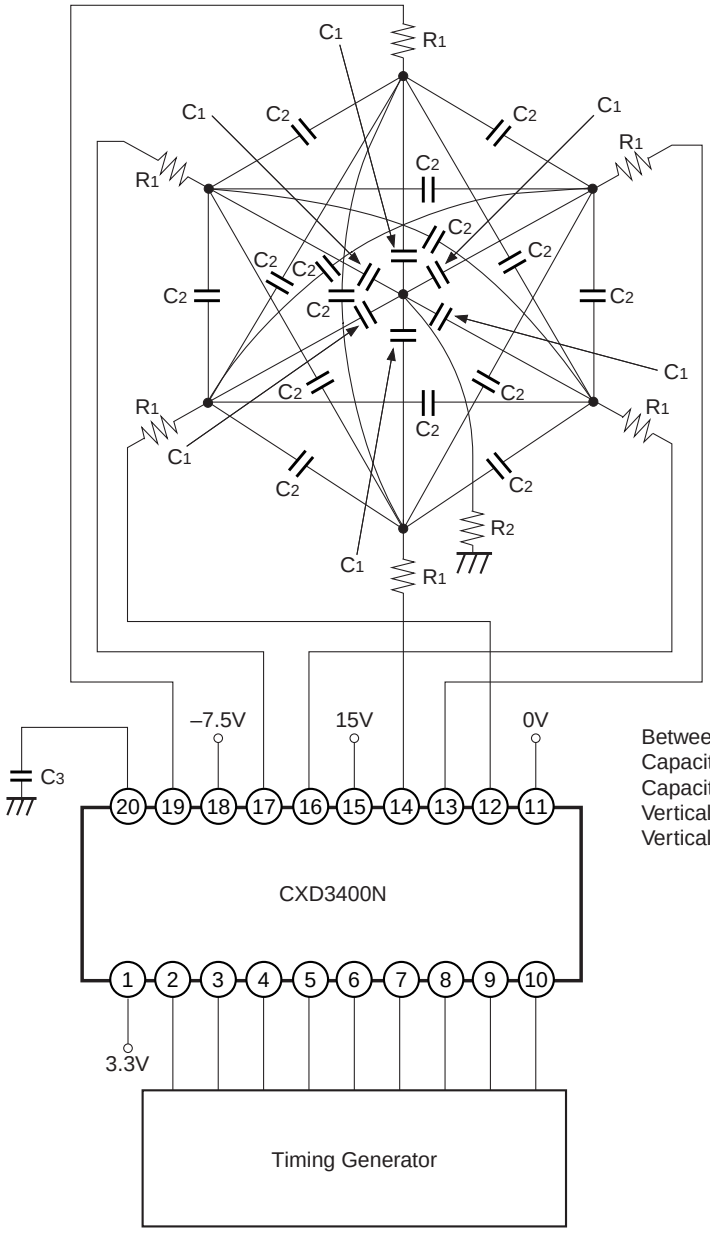
Switching Waveform



Noise on a Waveform

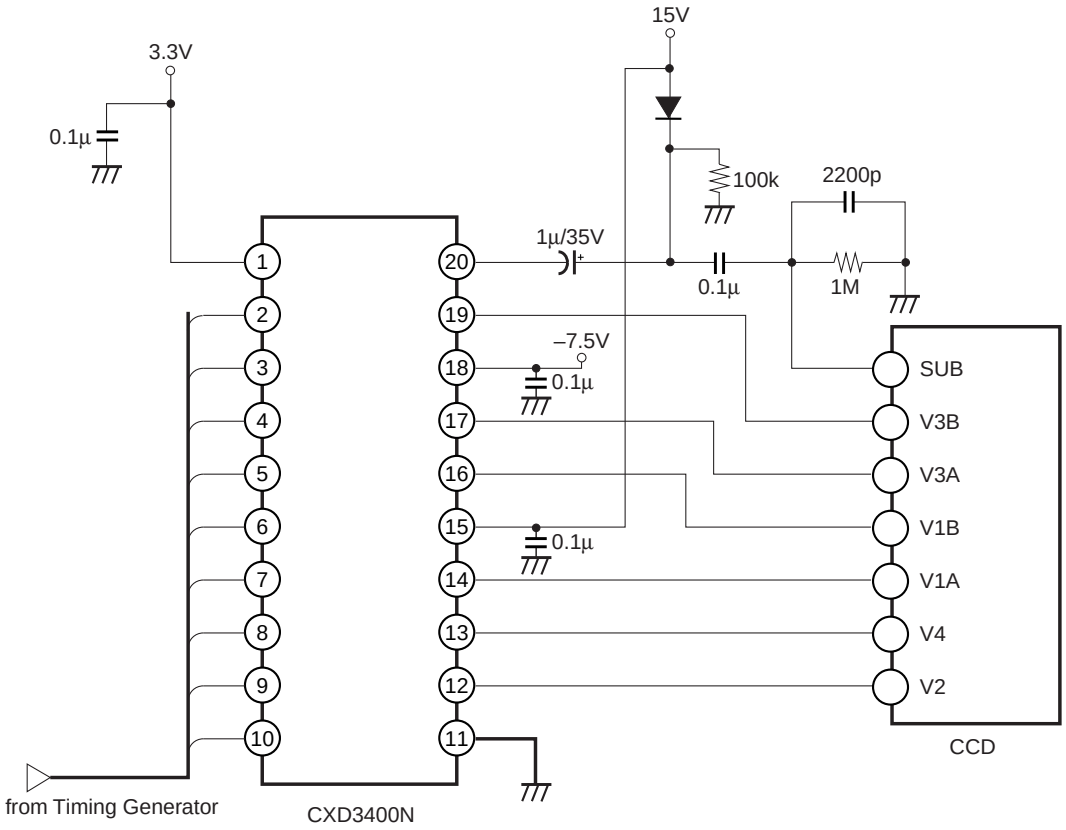


Measurement Circuit



Between vertical transfer clock and GND	C_1	3300pF
Capacitance between vertical transfer clocks	C_2	560pF
Capacitance between substrate clock and GND	C_3	820pF
Vertical transfer clock series resistor	R_1	30Ω
Vertical transfer clock ground resistor	R_2	10Ω

Application Circuit

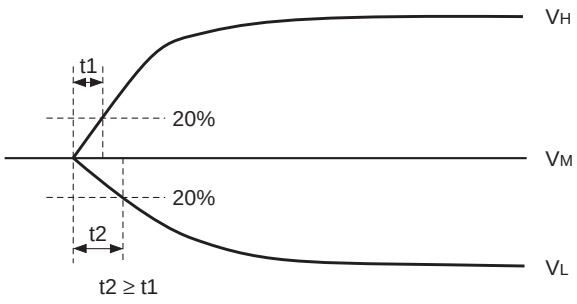


* See with drive circuit of CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

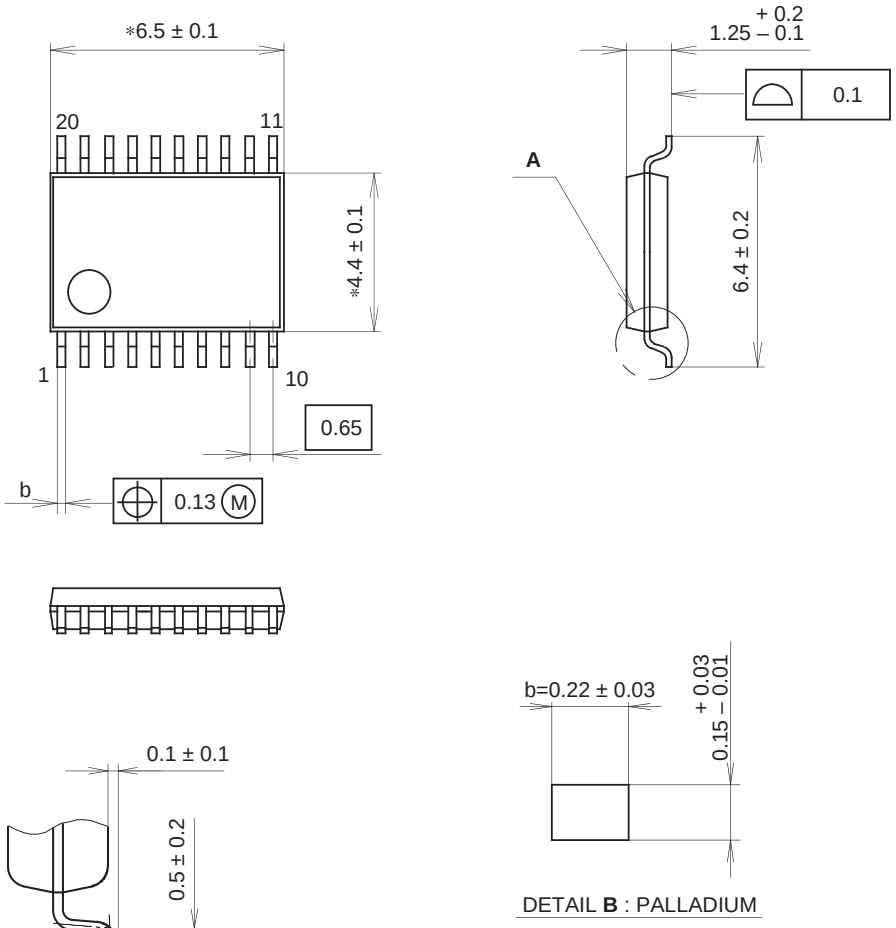
Note with Power-on Sequence

To protect CCD image sensor, rise two power supplies, V_L and V_H as follows.
Note that rise V_{DD} first.



Package Outline Unit: mm

20PIN SSOP (PLASTIC)



DETAIL **A**

DETAIL **B** : PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g